A NOVEL APPROACH FOR THE LARGE SIGNAL ANALYSIS AND OPTIMISATION OF MICROWAVE FREQUENCY DOUBLERS

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ABSTRACT

This paper describes a novel approach for the large signal analysis and optimization of microwave frequency doublers. A large signal lumped element model is used for an NE 71000 chip MESFET and a two level Harmonic Balance program employed in order to analyse and then optimize a target 'ideal' doubler. A practical circuit is then built in order to synthesize the 'ideal' doubler requirement. Agreement between experiment and theory is seen to be excellent.

INTRODUCTION

Fundamental mode MESFET oscillators can provide useful power at frequencies of the order of 20 GHz. Above this frequency the use of harmonic mixers and doublers is becoming more common. This paper describes a novel method for the optimum design of MESFET frequency doublers, which makes use of the special properties of the harmonic balance method of non-linear analysis.

To experimentally verify the method, a single ended doubler operating from 7 GHz to 14 GHz has been used as a demonstrator. A circuit model for the NE71000 GaAs MESFET chip which has been used in the circuit is presented.

The method described here is immediately transferable to multipliers of higher order, and to higher frequencies.

LARGE SIGNAL MODEL FOR NE71000

The large signal terminal characteristics of the MESFET chip (including bonding wires) are represented by the lumped circuit model shown in Figure 1. The circuit consists of linear components, and three principal non-linear terms, which are represented by the current generators I_D, I_G and I_B.

The element values for the circuit are found from:

(a) d.c. characteristic measurement
(b) d.c. terminal measurements described by Fukui[1].
(c) small-signal S parameter measurements.

Figure 2 shows the measured MESFET d.c. characteristics. These equations determine the main non-linearity, I_D. Using Fukui's method[1], parameters are obtained for I_G - the onset of increased gate current when the gate-source junction is forward biased, and for I_B - the injection of avalanche breakdown current at high drive voltages.

By combining the non-linear current sources with the linear circuit elements, a large-signal circuit for the NE71000 MESFET chip has been derived, Fig. 1.

HARMONIC BALANCE ANALYSIS METHOD

In Figure 3, the large-signal MESFET model is embedded in an external circuit. Z_1, Z_2 and Z_3 are linear elements describing bond wire effects etc. Z_g and Z_L represent source and load impedances; V_{GG}, V_{DD} represent d.c. bias voltages and V_G represents the external microwave input voltage to the circuit. Z_g, V_g and Z_L are the Thèvenin equivalents at a given frequency of complex external microwave circuits, incorporating lossy and/or dispersive lines, lumped components etc.

The circuit in Figure 3 may be partitioned into linear and non-linear sections: The resulting equations have the form

$$AV_G + BV_D = F_1(I_B,I_D,I_G);\quad I_D(V_G,V_D),\ I_B(V_G,V_D),\ I_G(V_G)$$

$$CV_G + DV_D = F_2(I_B,I_D,I_G) \qquad (1)$$

The terms A, B, C, D involve combinations of linear circuit admittances. Hence the left hand side of each equation represents linear circuit current. The right hand side of each equation involves the non-linear current terms I_B,I_D and I_G.

The principal periodic variables V_G and V_D can be represented in the time domain $V_G(t)$, $V_D(t)$, or in the frequency domain by their Fourier series expansions, truncated at a chosen harmonic, N.

Initially the values of the steady state Fourier components of V_G and V_D are estimated, using piecewise linear analysis. The corresponding $V_G(t)$ and $V_D(t)$ are found using the Discrete Fourier Transform (DFT). The non-linear current terms on the right hand side of the defining equations are evaluated in the time domain. The DFT enables the corresponding Fourier components

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to be equated to those evaluated from the linear terms on the left hand side. Four simultaneous equations result for each harmonic considered. The solution method uses an optimisation procedure to vary the Fourier coefficients of V_G and V_D until these equations are satisfied to within a given accuracy.

INITIAL DOUBLER DESIGN

The doubler was initially designed on the basis of matching at MESFET input and output terminals for maximum input power at 7 GHz and maximum output power at 14 GHz. The small-signal S parameters were employed for this purpose. Band-stop stubs were used to inhibit 7 GHz signals at the output port, and 14 GHz signals at the input port. The output power peaked at 8.4 dBm, with a multiplication gain of -3 dB.

IDEAL DOUBLER

Using the property of harmonic balance analysis, that at each harmonic the MESFET terminating impedances can be different, the 'ideal' doubler shown in Figure 4 can be analysed at a number of input r.f. drive levels. Optimizing , N_g, X_g and N_L, X_L enable the MESFET to be terminated in general Thevenin impedances, Z_g and Z_L while being driven at 7 GHz from a 50 ohm generator, and while feeding a 50 ohm load at 14 GHz. In this case the fundamental frequency is reflected at the MESFET output from a short-circuit, placed at a distance from the MESFET output which may be changed by varying . The other harmonic terminators at input and output are assumed in this instance to be ideal short-circuits. This ideal doubler provides a unique vehicle for studying the complex interactions within the MESFET.

OPTIMIZATION OF THE DOUBLER

The optimization was carried out using two optimization algorithms, one within the other.

In the outermost loop the values of the design variables N_g, Z_g, , X_L, N_L were varied in order to maximize the output power at the second harmonic for a given available input power at the fundamental frequency. The algorithm used was a Variable Metric (Quasi-Newton) algorithm, as implemented by the OPVM program from the OPTIMA subroutine library[5]. The updating formula used by this program is that due to Broyden, Fletcher, Goldfarb and Shanno. Divided differences were used to estimate first derivatives. To avoid the risk of ill-conditioning, the variables were scaled so that their values could be expected to be of order 1.0; no other special action was needed.

For each trial value of the design variables, the circuit was analysed by solving the non-linear equations (1), which were 26 in number. This required another optimization algorithm to minimise the sum of squares of the residual errors. The OPLS program from the OPTIMA library, based on a modified damped Newton-Raphson algorithm, was selected. Once again estimated first derivatives were used.

Despite the nonlinearity of the objective functions to be extremised at each level, the large number of complete optimizations carried out in the inner loop and the necessity of using estimated derivatives, no particular difficulties were encountered. The complete process required 25 minutes of CPU time on a VAX 8600 computer.

DOUBLER SYNTHESIS

The optimum values for the ideal doubler parameters were found to be
$N_g = 0.7$; $X_g = 46.5$; $= 55^o$; $N_L = 1.4$; $X_L = 25$.
The bias levels for the MESFET were $V_{ds} = 4$ V; $V_{gs} = 0$ V.

The use of the generalised matching sections in the ideal doubler configuration, simplifies microwave circuit synthesis.

The final doubler synthesised based on the ideal doubler exhibited a maximum conversion gain of 2.6 dB, with a maximum output power of 11 dBm. At an input power level of 7 dBm, the output power was 9.4 dBm with a conversion gain of 2.4 dB.

EXPERIMENTAL VALIDATION

The circuit shown in Figure 5 was constructed on RT-Duroid 5880 and was tested. In order to eliminate avalanche destruction of the NE71000 chip device a "backed off" bias level was used. Results are shown for a bias level of $V_{ds} = 3$V and $V_{gs} = -0.5$ V. This results in suboptimal multiplication gain when compared with the 'ideal' case, figure 7, -1.4 dB (c.f. 2.4 dB). At the 7 dBm drive level at which the optimum circuit was developed the multiplication gain is -1.6 dB. With the new bias condition the circuit was simulated and was shown to give poor agreement with the measured result. It was recognised that the effects of chip bond wires and the chip capacitors had been neglected in the analysis. To compensate for the bond wires an additional 0.5 nH inductance was added to the MESFET gate. The decoupling capacitors used (AVX: Accu Wave size 0403) were measured across the frequency range 7-14 GHz. With these additions to the analysis the agreement between practical results and theory is excellent, exhibiting a worst case deviation in predicted and measured multiplication gain of 0.6 dB over the drive range 5-12 dBm.

CONCLUSIONS

A novel method for MESFET doubler design, which employs the specific properties of the harmonic balance non-linear analysis method to achieve improved performance, has been presented. A multiplication gain of 2.4 dB has been predicted for a NE71000 chip MESFET doubler from 7 GHz to 14 GHz. This method will have application to multiplier design, with output frequencies in the 20-40 GHz range, where circuit losses will be

significant and multiplication gain, low. The practical circuit was tested, agreement with the theoretical predictions is excellent. The ideal multiplier concept described in the paper provides a mechanism for the closer study of internal MESFET operation with a variety of external loads. It has thus been shown that a nonlinear analysis tool with fine tuning optimization facility can be created which will operate in a computationally efficient way without the use of special computer coding techniques provided the doubler is represented as a multiport device terminated in ideal components.

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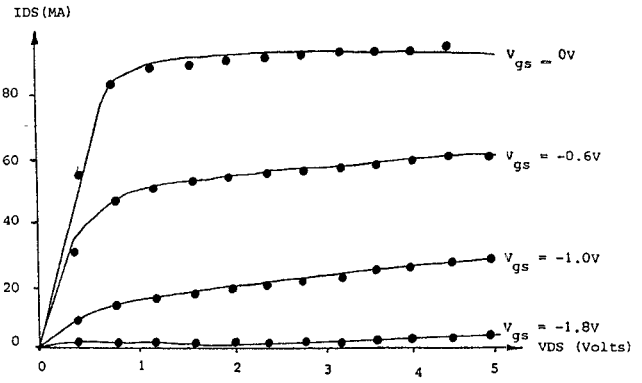


Tajima model

a = 13.78; b = -4.52; m = 7.41; p = 8.3 x 10^{-3}
Idsp = 132.5; Vdss = 1.58; Vb = 0.7; Vp = 1.61

Plus

$I_B = 2.07 \times 10^{-8} \{\exp(0.93V_g) - 1\}$

$I_C = 9.68 \times 10^{-12} \{\exp(30.3V_g) - 1\}$

Fig. 2 MESFET DC Characteristics (NE71000)
calculated o
measured —

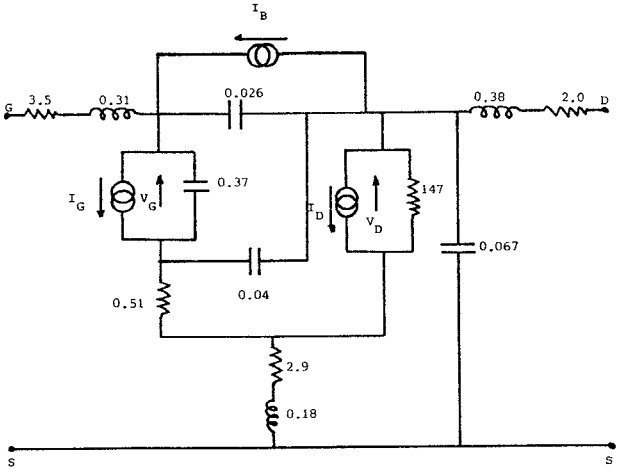


Fig. 1 LARGE-SIGNAL MODEL (NE71000)

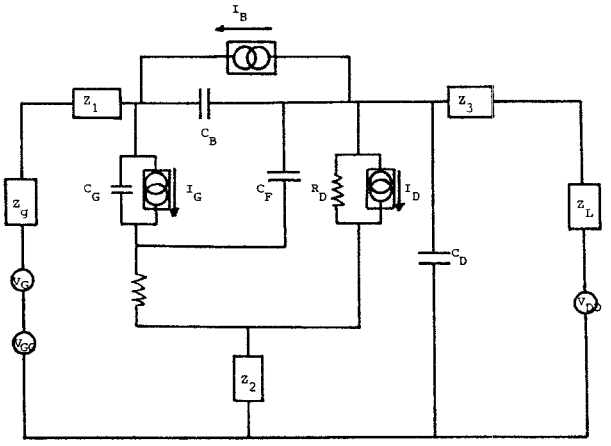


Fig. 3 PARTITIONED NONLINEAR MESFET MODEL

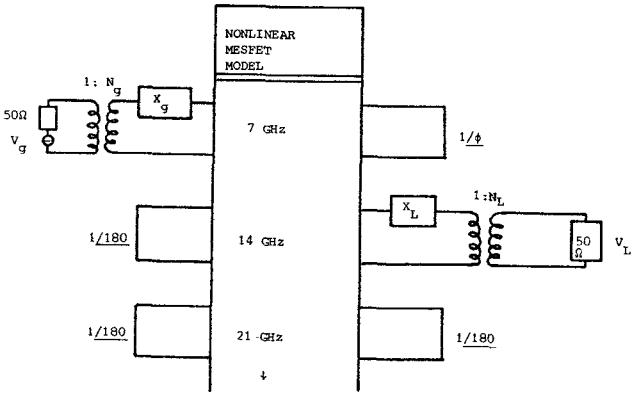
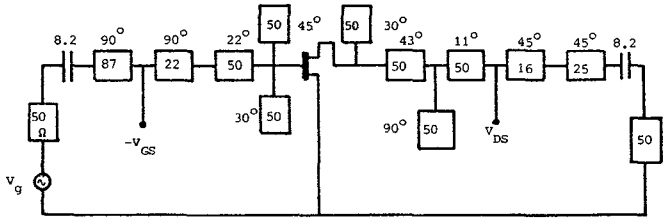
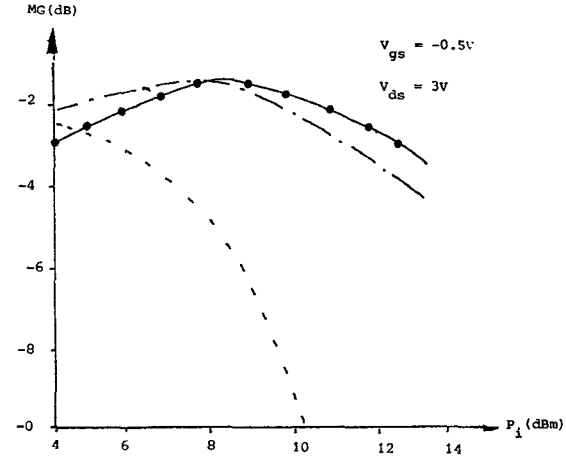


Fig. 4 IDEAL DOUBLER



(a) SYNTHESISED FINAL DOUBLER; P_i = 7dBm, N_g = 0.7; X_g = 46.5
Φ = 55°, X_L = 25, N_L = 1.4



(b) Doubler Performance

----- Initial Simulation
---- Simulation +0.5 nH gate inductance + capacitor model
—●●●— Measured Response

Fig. 5 Synthesised Doubler and Performance Characteristics